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PATENT APPLICATION AF

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IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): McBride

Confirmation No.: 7570

Application No.: 09/273,784

Examiner: Phan, T

Filing Date: March 22, 1999

Group Art Unit: 2123

Title: Method and Apparatus for Evaluating the Quality of Network Nodes

Mail Stop Appeal Brief-Patents
Commissioner For Patents
PO Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF

Sir:

Transmitted herewith is the Appeal Brief in this application with respect to the Notice of Appeal filed on *10/12/04*.

The fee for filing this Appeal Brief is (37 CFR 1.17(c)) $340.00.

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

( ) (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d) for the total number of months checked below:

( )	one month	$110.00
( )	two months	$430.00
( )	three months	$980.00
( )	four months	$1530.00

( ) The extension fee has already been filled in this application.

(*X*) (b) Applicant believes that no extension of time is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account ***08-2025*** the sum of ***$340.00***. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees. A duplicate copy of this sheet is enclosed.

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Signature: BFrench

Respectfully submitted,

McBride

By Daniel R. McClure

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BOARD OF PATENT APPEALS AND INTERFERENCES

In Re Application of:

John G. McBride

Serial No.: 09/273,784

Filed: March 22, 1999

For: METHOD AND APPARATUS FOR EVALUATING THE QUALITY OF NETWORK NODES

Group Art Unit: 2123
Examiner: Phan, T.

Confirmation No. 7570

TKHR Dkt. No. 50814-1470
HP Docket No. 10971308-1

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APPEAL BRIEF UNDER 37 C.F.R. §1.192

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Alexandria, Virginia 22313-1450

Sir:

This is an appeal from the decision of Examiner Thai Q. Phan, Group Art Unit 2128, mailed September 1, 2004, rejecting claims 1, 2, 8, 9, 15, and 16 in the present application and making the rejection FINAL.

I. REAL PARTY IN INTEREST

The real party in interest of the instant application is Hewlett-Packard Development Company, a Texas Limited Liability Partnership having its principal place of business in Houston, Texas.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

III. STATUS OF THE CLAIMS

The Office Action, however, rejected claims 1, 2, 8, 9, 15, and 16 under 35 U.S.C. § 103(a) as allegedly unpatentable over U.S. Patent 5,936,868 to Hall. Claims 3-7, 10-14, and 17-20 were only objected to as being dependent upon rejected base claims. The Office Action affirmatively stated that claims 3-7, 10-14, and 17-20 contained allowable subject matter.

IV. STATUS OF AMENDMENTS

No amendments have been made or requested since the mailing of the FINAL Office Action and all amendments submitted prior to the FINAL action have been entered. A copy of the current claims is attached hereto as Exhibit A.

V. SUMMARY OF CLAIMED SUBJECT MATTER

As embodied in claim 1, an apparatus is provided for evaluating a gate (e.g. reference numeral 138, FIG. 4B) to determine whether or not the gate has an acceptable immunity to noise. The apparatus comprises a computer configured to execute a rules

checker program (e.g., reference numeral 100, p. 10, lines 9-15), the rules checker program 100 receiving input relating to characteristics of a static gate (e.g., reference numeral 138, p. 17, lines 11-18) contained in the integrated circuit, the gate comprising at least two field effect transistors (e.g., reference numerals 139, 141, 142, and 143 of FIG. 4A), each field effect transistor having a width, the characteristics including the widths of the field effect transistors, the rules checker program 100 analyzing the widths (see e.g., Equation 1, p. 19) of the field effect transistors to determine whether or not the gate has an acceptable noise immunity (e.g., reference numeral 103, p. 10, lines 9-15).

As embodied in claim 2, the gate comprises at least one N field effect transistor and at least one P field effect transistor, the gate comprising at least first and second input terminals (e.g., terminals A and B of FIG. 4B) for receiving respective first and second input signals, the rules checker program processing the widths of the P field effect transistor and of the N field effect transistor to obtain a first numerical value relating to the widths (e.g., p. 19, lines 10-15 and p. 20, lines 12-17), the rules checker program utilizing the first numerical value to access first and second threshold values stored in a memory device (e.g., p. 20, line 18 through p. 21, line 10) in communication with the computer, the rules checker program determining noise levels on the inputs, the rules checker program comparing the determined noise levels with the threshold values read out of the memory device (e.g. p. 18, lines 16-24) and using the results of the comparison to determine whether or not the gate has an acceptable immunity to noise (e.g., p. 18, line 20 through p. 19, line 4).

As embodied in claim 8, a method for evaluating a gate (e.g., reference numeral 138, FIG. 4B) to determine whether or not the gate has an acceptable immunity to noise, the method comprising receiving input in a computer relating to characteristics of a static

gate (*e.g.*, reference numeral 138, p. 17, lines 11-18) contained in the integrated circuit, the gate comprising at least two field effect transistors (e.g., reference numerals 139, 141, 142, and 143 of FIG. 4A), each field effect transistor having a width, the characteristics including the widths of the field effect transistors; and analyzing the widths (e.g., Equation 1, p. 19) of the field effect transistors in the computer to determine whether or not the gate has an acceptable noise immunity (e.g., reference numeral 103, p. 10, lines 9-15), wherein the computer executes a rules checker program which analyzes the widths to determine whether or not the gate has an acceptable noise immunity.

As embodied in claim 15, a computer-readable medium containing a rules checker computer program 100, the computer program 100 evaluating a gate (e.g., reference numeral 138, FIG. 4B) to determine whether or not the gate has an acceptable immunity to noise, the gate comprising at least two field effect transistors (e.g., reference numerals 139, 141, 142, and 143 of FIG. 4A), each field effect transistor having a width, the characteristics including the widths of the field effect transistors, the program 100 comprising code which analyzes the widths (see e.g., Equation 1, p. 19) of the field effect transistors to determine whether or not the gate has an acceptable noise immunity.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1, 2, 8, 9, 15, and 16 stand rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over U.S. Patent 5,936,868 to Hall.

VII. ARGUMENT

Discussion of Rejection of Claims 1, 8, and 15

As summarized above, the present application is directed to methods and apparatus for evaluating a gate of an integrated circuit to determine whether or not the gate has acceptable immunity to noise. The apparatus comprises a computer configured to execute a rules checker program, which receives input relating to characteristics of a static gate contained in the integrated circuit. The gate comprises at least two field-effect transistors (FETs). Each FET has a width and the characteristics received in the input to the rules checker program include the widths of the field effect transistors. The rules checker program analyzes the widths of the FETs to determine whether or not the gate has an acceptable level of noise immunity.

Each gate typically comprises a plurality of FETs, usually at least one NFET and at least one PFET, and input terminals for receiving input signals. The rules checker program processes the widths of the PFETs and NFETs to obtain at least a first numerical value relating to the widths. The rules checker program utilizes the first numerical value to access one or more threshold noise-level values from a memory device in communication with the computer. The rules checker program determines noise levels on the inputs, either through calculation or simulation. The rules checker program compares the determined noise levels with the threshold values and uses the results of the comparison to determine whether or not the gate has an acceptable immunity to noise.

As embodied in independent claim 1, independent claim 1 recites:

> 1. An apparatus ***for evaluating a gate to determine whether or not the gate has an acceptable immunity to noise***, the apparatus comprising:
>
> a computer configured to execute a rules checker program, the rules checker program receiving input relating to characteristics of a static gate contained in the integrated circuit, the gate comprising at least two field effect transistors, each field effect transistor having a width, the characteristics including the widths of the field effect transistors, ***the rules checker program analyzing the widths of the field effect transistors to determine whether or not the gate has an acceptable noise immunity***.

(*Emphasis added.*) Applicant respectfully traverses the rejection of independent claim 1 for at least the reason that the cited art fails to disclose or teach at least the features emphasized above. The rejection of claims 8 and 15 should be overturned for similar reasons, as those claims embody similar (distinguishing) features.

The Office Action alleged that Hall teaches these features (or an obvious variant thereof). Applicant respectfully disagrees. In this regard, Hall is directed to a system and method for converting an integrated circuit design for an upgraded process. Specifically, Hall is directed to a system and method that automates the re-design of an integrated circuit for an updated manufacturing process. In the process of Hall, multiple downward size scalings are

first performed (to downward scale contacts and vias) before performing an upward size scaling.

Relevant to claimed features of the present application, however, the system and method of Hall does not teach an analysis or determination of noise immunity, as claimed by the presently pending claims. In fact, the only reference to, or acknowledgement of, noise in the Hall patent is in the context of a "noise ratio." Specifically, this noise ratio refers to a noise ratio between the original manufacturing process and the updated manufacturing process. If the original circuit design was subject to a certain level of noise, this level may differ in the update process, based on the change in dimensional scales between the original design and the updated design. This difference is referred to in Hall as a noise ratio. (See, e.g., col. 4, lines 46-57).

Returning to specific features defined in independent claim 1 (as well as independent claims 8 and 15), claim 1 specifically defines "***the rules checker program analyzing the widths of the field effect transistors to determine whether or not the gate has an acceptable noise immunity***." This element is neither taught nor suggested by Hall. It appears that the Office Action has confused certain teachings of the Hall patent, in applying this reference to reject claim 1 of the present application. To illustrate, Applicant notes with emphasis the teaching with Hall at col. 4, lines 37-56, which states:

> Yet another important aspect of the invention relates to the treatment of the supply rails. In other words, the method may further comprise the step of selectively performing a fifth upward ***size scaling on the mask data in at least one dimension to scale up at least one of the power supply rails***. The step of selectively performing the fifth upward scaling preferably comprises displaying and viewing an image of the IC design, and selecting the power supply rails based on displaying and viewing the image. Moreover, the step of the fourth upward size scaling for the power supply rails preferably comprises the step of determining a scaling factor based on a desired voltage noise ratio between the original process and the updated process.
>
> ***In another embodiment relating to the treatment of the supply rails, the method includes determining a desired width upward scaling factor***

> ***based on a desired voltage noise ratio between the original process and the updated process, and selectively adding at least one additional parallel supply rail based upon determining that the desired width upward scaling factor is greater than about two.***

(*Emphasis added.*) Thus, while this portion of Hall mentions the terms "width" and "noise," it is not referring to the FET width or noise immunity, as claimed in claim 1. Instead, the "width" that this location of Hall is referring to is a dimensional width for applying an upscaling factor (while holding a length of a second dimension constant during the upscaling). Likewise, the noise that Hall is referring to us a noise ratio between the power supply rails of an original process and an updated process (where the update process results from the collective downscaling and upscaling steps of the method of Hall).

The Office Action also referenced column 7 line 21 through column 8, line 25 in support of its application of Hall to the claims. There, the description in Hall makes reference to the channel width and length of a MOS device. Specifically, Hall states that "additional intervention" may be required to ensure that the scaling does not reduce a channel length to a smaller (or shorter) size that that which is allowed by the fabrication process (col. 7, lines 21-24). Stated another way, Hall recognizes that, if the mathematical portion of the scaling process would generate a circuit design requiring smaller dimensions than the fabrication process would support, then additional intervention would be required. This, however, is unrelated to the claimed feature of claim 1, which has been emphasized.

The Office Action further references the teaching of col. 8, lines 12-26 as allegedly teaching "the design rule checker program is to check transistor noises such as transient noise, noise levels, etc." Applicant respectfully disagrees. This portion of Hall specifically states:

> A plot of Vss (ground) metal ratio (w_x /w_n) for a CMOSN part converted to a CMOSX (0.8 μM) part is shown in FIG. 6 for Vdd_n =5.0 V and ξ=1. Similarly, FIG. 7 shows the requirements for Vdd distribution. Note that the conversion of a CMOSN part in a 5V application to a CMOSX (0.8 mm) part in a 3.3V application requires no change to either the ***Vdd (power) or***

> ***the Vss (ground) distribution width if the allowable noise levels on the distributions in the two cases are identical.*** If the maximum operating voltage of the converted IC is limited to 3.3V, no power or ground metalization adjustment needs to be made in the conversion process; however, if operation at 5V is required to be maintained, then an adjustment is required as shown in the cell 25A, 25B and 25C of FIGS. 5A, 5B and 5C, respectively.

(*Emphasis added.*)

This portion of Hall (along with the equations at the bottom of col. 7) teaches an assessment of MOS channel width/length ratios in comparison to the ratio of original process to the updated process to determine whether a distribution width of either Vdd (power) or Vss (ground) needs to be changed. That is, Hall does not teach or disclose the determination of whether a gate is susceptible to noise immunity by evaluating the widths of the field effect transistors that comprise the gate. Instead, Hall teaches only the evaluation of circuit and device parameters to determine whether a noise ratio (resulting from a circuit scaling conversion) is within acceptable limits, or whether a dimensional limitation in the scaling process will need to be changed.

Finally, the Office Action (see first paragraph of page 3) cites Equation 3 of col. 7 (approx. lines 58-60) as allegedly disclosing "analyzing the widths of gate channel to determine noise generated in MOSFET." Applicant respectfully traverses this interpretation of Equation 3 and application of Hall. As specifically stated in Hall (see. col. 7, lines 45-47) "Equation 3 relates current switching transients to <u>distribution noise in the form of a ratio between the two IC fabrication processes</u>." (*Emphasis added.*)

Simply stated, Hall does not teach or disclose ***analyzing the widths of the field effect transistors to determine whether or not the gate has an acceptable noise immunity***, as is specifically claimed by independent claims 1, 8, and 15. In fact, the Office Action even

admits that "Hall does not expressly disclose noise immunity in the design rule checking as claimed." (Office Action, p. 3, lines 8-9).

Notwithstanding, the Office Action alleges:

> Practitioner in the art at the time the invention was made would have found Hall disclosure of design rule checking for checking acceptable noise level or allowable noise as above implies the feature of noise immunity as claimed such that circuit under operation is immune to noise, or certain allowable noise levels.

(Office Action, p. 3, lines 10-13). This statement is nothing more than a bare, subjective conclusion, and is not supported by any tangible teaching or objective reference. As such the rejection is inappropriate and should be withdrawn. Stated another way, this same subjective, conclusive reasoning could be used to reject any claim. In essence, anytime the prior art does not teach a claimed feature, an Examiner could simply conclude that the feature is obvious. The law surrounding rejections under 35 U.S.C. § 103(a) developed to prevent just this time of subjectivity on the part of the Patent Office. As the conclusion of the Examiner is unsupported, the rejection is misplaced and should be overturned.

For at least the several reasons described above, the rejections to independent claim 1 should be overturned. As independent claims 8 and 15 embody similar distinguishing features, the rejection of those claims should be overturned for the same reasons.

Discussion of Rejection of Claims 2, 9, and 16

The Office Action also rejected claims 2, 9, and 16 under 35 U.S.C. § 103(a) as allegedly unpatentable over U.S. Patent 5,936,868 to Hall. The rejection stated:

> As per claim 2, Hall discloses transistor design parameters and reading design parameters such as transistor channel length, gate width, channel widths, and the likes for checking design rule as claimed. Such transistor circuit design in static gate under rule checking would include for example inverter gate, p-channel and n-channel transistor, CMOS channel

> parameters, design parameters, etc. as well-known in transistor circuit design, and the rule checking of the gate circuit statically verifies device characteristics and performance analysis such as susceptibility for noise levels, acceptable transient noise in a specified design operation bound within thresholds values as known in MOS and CMOS of the circuit design (col. 7, line 34 to col. 8, line 26).

This rejection, however, fails to address all of the features of claim 2 (and likewise, claims 9 and 16). Claim 2 specifically recites:

> 2. The apparatus of claim 1, wherein the gate comprises at least one N field effect transistor and at least one P field effect transistor, the gate comprising at least first and second input terminals for receiving respective first and second input signals, the rules checker program ***processing the widths of the P field effect transistor and of the N field effect transistor to obtain a first numerical value*** relating to the widths, the rules checker program ***utilizing the first numerical value to access first and second threshold values stored in a memory device*** in communication with the computer, the rules checker program ***determining noise levels on the inputs***, the rules checker program ***comparing the determined noise levels with the threshold values read out of the memory device and using the results of the comparison to determine whether or not the gate has an acceptable immunity to noise***.

Simply stated, claim 2 expressly defines features that were wholly unaddressed by the Office Action and which are not disclosed in the cited reference to Hall. For example, claim 2 calls for processing PFET and NFET widths to obtain a "first numerical value," utilizing that first numerical value "to access first and second threshold values stored in a memory device," "determining noise levels on the inputs," and "comparing the determined noise levels with the threshold values" to "determine whether or not the gate has an acceptable immunity to noise."

As these features are not disclosed in Hall (and indeed are not even alleged by the Office Action), the rejection of claim 2 is misplaced and should be overturned. The claimed features and rejections of claims 9 and 16 are similar, and should be overturned for the same reasons.

CONCLUSION

Based upon the foregoing discussion, Applicants respectfully requests that the Examiner's final rejection of claims 1, 2, 8, 9, 15, and 16 be overruled by the Board, and that the application be allowed to issue as a patent with all pending claims.

Please charge Hewlett-Packard Company's deposit account 08-2025 in the amount of $340 for the filing of this Appeal Brief. No additional fees are believed to be due in connection with this Appeal Brief. If, however, any additional fees are deemed to be payable, you are hereby authorized to charge any such fees to deposit account No. 08-2025.

Respectfully submitted,

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VIII. CLAIMS - APPENDIX

1. An apparatus for evaluating a gate to determine whether or not the gate has an acceptable immunity to noise, the apparatus comprising:

a computer configured to execute a rules checker program, the rules checker program receiving input relating to characteristics of a static gate contained in the integrated circuit, the gate comprising at least two field effect transistors, each field effect transistor having a width, the characteristics including the widths of the field effect transistors, the rules checker program analyzing the widths of the field effect transistors to determine whether or not the gate has an acceptable noise immunity.

2. The apparatus of claim 1, wherein the gate comprises at least one N field effect transistor and at least one P field effect transistor, the gate comprising at least first and second input terminals for receiving respective first and second input signals, the rules checker program processing the widths of the P field effect transistor and of the N field effect transistor to obtain a first numerical value relating to the widths, the rules checker program utilizing the first numerical value to access first and second threshold values stored in a memory device in communication with the computer, the rules checker program determining noise levels on the inputs, the rules checker program comparing the determined noise levels with the threshold values read out of the memory device and using the results of the comparison to determine whether or not the gate has an acceptable immunity to noise.

3-7. Not appealed.

8. A method for evaluating a gate to determine whether or not the gate has an acceptable immunity to noise, the method comprising the steps of:

receiving input in a computer relating to characteristics of a static gate contained in the integrated circuit, the gate comprising at least two field effect transistors, each field effect transistor having a width, the characteristics including the widths of the field effect transistors; and

analyzing the widths of the field effect transistors in the computer to determine whether or not the gate has an acceptable noise immunity, wherein the computer executes a

rules checker program which analyzes the widths to determine whether or not the gate has an acceptable noise immunity.

9. The method of claim 8, wherein the gate comprises at least one N field effect transistor and at least one P field effect transistor, the gate comprising at least first and second input terminals for receiving respective first and second input signals, the analyzing step being performed by the rules checker program further comprising the steps of:

processing the widths of the P field effect transistor and of the N field effect transistor to obtain at least a first numerical value relating to the widths;

utilizing the first numerical value to access first and second threshold values stored in a memory device in communication with the computer;

determining noise levels on the input terminals; and

comparing the determined noise levels with the threshold values read out of the memory device and using the results of the comparison to determine whether or not the gate has an acceptable immunity to noise.

10-14. Not appealed.

15. A computer-readable medium containing a rules checker computer program, the computer program evaluating a gate to determine whether or not the gate has an acceptable immunity to noise, the gate comprising at least two field effect transistors, each field effect transistor having a width, the characteristics including the widths of the field effect transistors, the program comprising:

code which analyzes the widths of the field effect transistors to determine whether or not the gate has an acceptable noise immunity.

16. The computer-readable medium of claim 15, wherein the gate comprises at least one N field effect transistor and at least one P field effect transistor, the gate comprising at least first and second input terminals for receiving respective first and second input signals, the code comprising:

a first code segment which processes the widths of the P field effect transistor and of the N field effect transistor to obtain a first numerical value relating to the widths;

a second code segment which utilizes the first numerical value to access first and second threshold values stored in a memory device in communication with the computer;

a third code segment which determines noise levels on the input terminals; and

a fourth code segment which compares the determined noise levels with the threshold values read out of the memory device and uses the results of the comparison to determine whether or not the gate has an acceptable immunity to noise.

17-20. Not appealed.

IX. EVIDENCE - APPENDIX

None.

IX. RELATED PROCEEDINGS- APPENDIX

None.